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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/401,765	09/23/1999	PHILIP J. CALAMATAS	WAB98553	5126

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EXAMINER
GOSSAGE, GLENN A

ART UNIT	PAPER NUMBER
2187	13

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/401,765	CALAMATAS, PHILIP J.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2003 and 12 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *30 January 2003* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --PASSENGER TRANSIT CAR INCLUDING A SELF-LOCKING MEMORY OR BUS HOLD CIRCUIT FOR A TRI-STATE DATA BUS-- is suggested (see claim 11, lines 1 and 13, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

2. The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). It appears in line 1, "programmable system and" should be changed to --passenger transit car such as a railcar including-- for clarity and completeness (note claim 11, line 1, e.g.). Also, one or two sentences or phrases should be added describing additionally claimed and disclosed features. [For example, in line 7, after "circuit", insert --to reduce the effects of electrical noise on the data bus-- (note page 4, lines 10-13, e.g.). Additionally, in line 9, before "thresholds," insert --upper and lower-- (see claim 11, lines 21-22, e.g.]

Appropriate correction is required. See MPEP § 608.01(b).

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on January 30, 2003 have once again been disapproved by the Examiner.

The drawings are once again objected to because in Figure 1B (as proposed), the addition of the "boxes" labeled "DSP" and "CPLD" while deleting the labels "(DSP CHIP)" and "(OTHER CHIPS)" does not appear to be clearly supported by the disclosure as originally filed and may constitute NEW MATTER. [Should the (added) labels DSP and CPLD be placed within their respective "boxes" (see the originally filed drawings), or the "boxes" labeled DSP and CPLD be placed inside their respective larger "boxes" adjacent to the labels "(DSP CHIP)" and "(OTHER CHIPS)?"]

The remaining drawing changes submitted in the response filed January 30, 2003 are acceptable but should be resubmitted for proper approval and entry by the Examiner.

It is also noted here that new Figures 3A-12E added in the amendment filed January 30, 2003 have not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in these Figures.

Applicant is again REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

The drawings are also objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "complex programmable logic device" of claim 13 must be shown or the features canceled from the claims. No new matter should be entered. [In this regard, note the disapproval above of the proposed drawing corrections filed January 30, 2003.]

4. It is once again noted here that the specification, particularly the material added or incorporated from the provisional application at the end of the specification, has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 8, line 9, it appears --provisional-- should be inserted before "application" for clarity and consistency (see lines 6-7, as well as page 1, line 3, e.g.).

Similarly, on page 12, line 15, it appears --provisional-- should be inserted before "patent" for clarity.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 11, lines 3 and 10, it appears "first" should be deleted (note that there is no "second" plurality of solenoids). Similarly, it appears "second" in lines 4 and 10, "third" in lines 5 and 11, and "fourth" in line 8, should be deleted for clarity. Also, it appears lines 23-27 should be deleted as being repetitive (note lines 18-22).

In claims 12 and 13, line 2, it appears "self-locking memory circuit" reads more clearly here as --passenger transit car-- (the DSP and CPLD do not appear to be a part of the "self-locking" memory circuit).

Also in claim 13, line 2, it appears "11" should be --12-- [note the references to the ("said") tri-state data bus, central processing unit and digital signal processor].

Appropriate correction is required.

5. Claims 11-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, and therefore its dependent claims, it is not entirely clear how the self-locking memory circuit or the tri-state bus having multiple bit lines is connected or related, if at all, to the electrical control unit, including the motherboard and daughter boards, or to the other elements in the claim.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (see Fig. 3A and page 13, line 1 to page 14, line 23 of the present specification, for example) in view of Buch.

With respect to claim 11, applicant's admitted prior art discloses that a passenger transit car, such as a railway passenger car or railcar, including a car drive motor, a plurality of solenoids, a plurality of mechanical switches, and a plurality of motors for moving doors on the passenger transit car, was known in the art at the time the claimed invention was made. See, for example, page 13, line 1 to page 14, line 23 and Figure 1 of the present disclosure.

As one of ordinary skill in the art would readily appreciate, the passenger transit car or railcar also includes an electrical control unit for controlling operation of the solenoids, switches and motors to operate the doors and other parts of the railcar, the control unit having a main board or "motherboard" and a plurality of other boards. The boards have mounted thereon a plurality of integrated circuits or "chips" such as a microcontroller or other signal processing circuitry connected by lines or buses to process signals necessary to control the doors and other parts of the railcar in a well known manner.

However, the passenger transit car of applicant's admitted prior art does not include a "self-locking" data bus hold or memory circuit connected to respective bit or data lines of a data bus, so as to hold the values on the data bus at a particular value and prevent the data bus from "floating" to undetermined values and possibly causing erroneous operation by a central processing unit (CPU) or other signal processing circuitry coupled to the data bus.

Buch discloses a "self locking" memory or bus latching circuit for a tri-state data bus having multiple bit or data lines, the memory or latching circuit including a non-inverting buffer or amplifier (note 64, 66 together, e.g., in Figure 5, as well as column 5, lines 58-62) for connection to one of the bit or data lines, and a resistor (68 in Fig. 5, e.g.) having a predetermined electrical resistance connected across the buffer or amplifier. [Note that while two inverters are shown in Figure 5, Buch also teaches that a non-inverting amplifier may be used in place of the pair of inverters 64, 66 (see column 5, lines 60-62, e.g.)] The resistance value may be chosen to adjust the thresholds at which the circuit will change state. In this manner, the self-locking memory or bus latching circuit has upper and lower "threshold" voltage thresholds that cause the non-inverting buffer chip or latching circuit to change states when a level of voltage applied to the chip and the resistor "passes through" one of the thresholds. The memory or latching circuit is "self-locking" and does not change state until a voltage is again applied to the data bus which "passes through" one of the thresholds. See column 5, lines 31-35; column 5, line 56 to column 6, line 2; column 6, line 61b to column 7, line 5; and Figure 5, for example.

The memory or bus latching circuit maintains or stores the level of data on the bus until a

subsequent data or voltage level of a sufficient amount is driven onto the data bus. In this way, different components of the computer system operating at different rates may communicate over the data bus, while maintaining data integrity and allowing faster bus switching times.

Buch also teaches that the bus may be a communication link between one or more computer components, and that the various components may comprise large scale integrated circuits or chips (see column 1, lines 14-39, e.g.). Bush also teaches that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to utilize a "self-locking" memory or hold circuit as taught by Buch, on the signal lines in the passenger transit railcar of applicant's admitted prior art, in order to maintain or store the level of data on the bus until a subsequent data or voltage level of a sufficient amount is driven onto the data bus so that different components or chips operating at different rates may communicate over a data bus, while maintaining the integrity of the data on the bus and allowing faster bus switching times.

Also, with respect to claim 12, Buch does not specifically teach that the large scale integrated circuits or chips or components of the system are comprised of a CPU and a "digital signal processor" (DSP) having different rates at which they operate in performing their respective functions. However, Bush does teach that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.), and

it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize the self-locking memory or bus latching circuit of Buch with large scale integrated circuit components or chips such as digital signal processors, which are components used commonly with data buses, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow fast and error free communication between the different chips.

It would have been obvious to use such data bus latching circuits because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a system using "computer" components (note column 1, line 55 to column 2, line 64, e.g.).

In this regard, applicant's arguments filed January 30, 2003, insofar as applicable to the new grounds of rejection, have been considered but are not persuasive. It is believed applicant's arguments have been addressed in the preceding paragraphs.

Also, the argument that "(it) is an advantage of the present invention that the electrical noise generated by motors, solenoids and switches can be tolerated by the self-locking circuit" (response at page 6) is not persuasive since the self-locking bus hold circuit of Buch also provides the advantage of making a circuit or a bus tolerant to electrical noise. The "thresholds" in Buch may be adjusted so that the self-locking bus hold circuit changes states at desired voltage

level so that small amounts of electrical noise on the data bus will not cause the self-locking bus hold circuit and data bus to change states. Buch also teaches that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips, and also teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (again note column 1, line 55 to column 2, line 64, e.g.).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Buch as applied to claims 11-12 above, and further in view of Chiang et al.

With respect to claim 13, applicant's admitted prior art in view of Buch discloses a passenger transit car including motors, solenoids, switches and appropriate control circuits or chips, as well as a tri-state data bus and a plurality of "self-locking" data bus latching or memory circuits connected to respective bit or data lines of the data bus as in the present invention (see numbered

paragraph 6 above).

Buch teaches that the "self locking" data bus latching circuit may used so that different components of a system operating at different rates may communicate over a data bus, while maintaining data integrity and allowing faster bus switching times. Buch further teaches that the bus may be a communication link between one or more computer components, and that the various components may include "nodes" comprised of large scale integrated circuits or chips including a central processing unit or CPU (see column 1, lines 14-39, e.g.), but does not specifically teach that the large scale integrated circuits or chips or components to which the bus hold circuit is connected include a complex programmable logic device (PLD) or CPLD. However, as noted above, Bush does teach that the components may comprise any typical components used commonly with data buses.

Chiang et al similarly discloses a bus hold circuit including a resistance and a non-inverting amplifier, and also teaches that the bus hold circuit may be used with busses coupled to integrated circuits, specifically teaching that the bus hold circuit may be used with complex programmable logic devices (CPLDs) to hold or latch the data on the bus (see column 1, lines 13-54 and Figure 1, e.g.).

Accordingly, it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize large scale integrated circuit components or chips such as complex programmable logic devices, as taught by Chiang et al, which CPLDs are commonly used with data buses, in conjunction with the self-locking circuits in the passenger

transit car of applicant's admitted prior in view of Buch, as discussed above, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips, including CPUs and CPLDs. It would have been obvious to use such data bus latching circuits because Buch and Chiang et al teach that the states on the data bus may be reliably held between "drives" or when the bus is not being driven but can be overwritten or overcome by the drivers to obtain a new state, and because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components (note column 1, line 55 to column 2, line 64 of Buch, e.g.), particularly one using chips such as CPUs, DSPs and CPLDs.

The reduction or avoidance of delays due to transitions in a tri-state bus and accompanying improvement in data bandwidth and integrity, coupled with the teaching of using the self-locking data bus circuit in conjunction with typical computer components and large scale integrated circuits commonly used with data buses, as specifically taught by Buch, provide ample motivation and suggestion to utilize the self-locking data bus circuits of Buch in conjunction with computer components commonly used with data buses such as DSPs and CPLDs. One of ordinary skill in the art at the time the claimed invention was made would have found it readily obvious to utilize "typical" components such as a digital signal processor (which is merely a processor which processes digital signals) and a ("complex") programmable logic device, both of which are large scale integrated circuit components or chips commonly used with data buses,

particularly in light of the specific teachings of Chiang et al.

In short, the combined teachings of the references renders obvious a structure on which applicant's claims read, and thus the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the combined teachings of the references.

8. In this regard, applicant's arguments filed January 30, 2003, insofar as applicable to the new grounds of rejection, have been considered but are not persuasive. It is believed applicant's arguments have been addressed in the preceding paragraphs.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final

action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238	(After Final Communications)
(703) 746-7239	(Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187